20.8GSPS / 15.2GSPS / 12GSPS 12b Analog-To-Digital Converter (ADC)

1 Characteristics

- Resolution: 12-bit, NO missing code
- Sampling Rate:
  CAE2200s : 20.8 GSPS (single), 10.4 GSPS (dual), 5.2 GSPS (quad)
  CAE2300s : 15.2 GSPS (single), 7.6 GSPS (dual), 3.8 GSPS (quad)
  CAE2400s : 12 GSPS (single), 6 GSPS (dual), 3 GSPS (quad)
- # Channels: 1 / 2 / 4
- Input Signal Range [$V_{pp,diff}$]: 0.8V (typ) , 1V (max)
- Analog Input Bandwidth (-3dB): TBD
- Code error rate: < 10^{-15}
- Integral-Nonlinearity INL @ 180 MHz :
  CAE2200s: -2.7 / +2.7 LSB
  CAE2300s: -1.5 / +1.4 LSB
  CAE2400s: -1.6 / +1.8 LSB
- Differential-Nonlinearity DNL @ 180 MHz :
  CAE2200s: -0.52 / +0.60 LSB
  CAE2300s: -0.44 / +0.67 LSB
  CAE2400s: -0.52 / +0.63 LSB
- SNR @ 1GHz (2200s/2300s) 1.09 GHz (2400s):
  CAE2200s: 49.4 dBFS (-10dBFS), 47.6 dBFS (-1dBFS)
  CAE2300s: 51.1 dBFS (-10dBFS), 50.2 dBFS (-1dBFS)
  CAE2400s: 51.5 dBFS (-10dBFS), 50.8 dBFS (-1dBFS)
- SFDR @ 1GHz (2200s/2300s) 1.09 GHz (2400s):
  CAE2200s: 68.7 dBc (-10dBFS), 63.8 dBc (-1dBFS)
  CAE2300s: 70.6 dBc (-10dBFS), 66.9 dBc (-1dBFS)
  CAE2400s: 65.6 dBc (-10dBFS), 68.7 dBc (-1dBFS)
- ENOB @ 1GHz (2200s/2300s) 1.09 GHz (2400s):
  CAE2200s: 7.9b (-10dBFS), 7.6b (-1dBFS)
  CAE2300s: 8.2b (-10dBFS), 8.0b (-1dBFS)
  CAE2400s: 8.2b (-10dBFS), 8.1b (-1dBFS)
- 32 lanes JESD204B output, with maximum lane rate of 15.0 Gbps, support 8b/10b coding, and support subclass 1
- Embedded Programmable DDC: Programmable FIR banks with decimation ratio of 1x,2x,3x,4x,6x,8x, 12x,16x,24x,32x,48x, and 64x for real output, or with decimation ratio of 2x,4x,6x,8x,16x,24x,32x, 48x,64x,96x,128x for complex I/Q output.
  The 48-bit NCO is embedded in each DDC and support fast frequency hopping
- Clamp diode protection in analog differential input
- Temperature-Tracked diode embedded
- Junction temperature: -40 to 115°C
- Low Power Consumption:
  CAE2200s : 6.0W (single / dual) , 6.34W (quad)
  CAE2300s : 5.3W (single / dual) , 5.62W (quad)
  CAE2400s : 4.8W (single / dual) , 5.0W (quad)
- Package: FCBGA484 (19mm x 19mm)

2 Applications

- Oscilloscope and Wideband digitizer
- Broadband communications
- High-Speed Data Acquisition Unit
- Communication Tester (802.11ad, 5G)
- Wireless Software Defined Ratio (SDR)
- Spectrometer

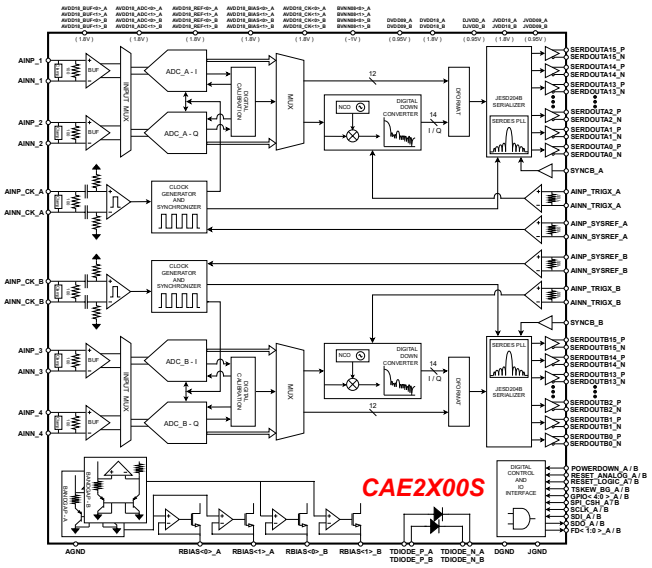
3 General Descriptions

CAE2200s / CAE2300s / CAE2400s is a 12b RF Analog-To-Digital Converter (ADC) with maximum sampling rate of 20.8GSPS / 15.2GSPS / 12GSPS in single channel mode, and with maximum sampling rate of 10.4GSPS / 7.6GSPS / 6GSPS in dual channel mode, and with maximum sampling rate of 5.2GSPS / 3.8GSPS / 3GSPS in quad channel mode.

The single / dual / quad channel mode can be configured by SPI setting, can be developed by flexible hardware to support multi-channels or wide instantaneous bandwidth applications.

CAE2200s / CAE2300s / CAE2400s adopt high speed JESD204B output interface, with the operating junction temperature of -40 to 115°C, and the package of Flip-Chip BGA 484 pins (19mm x 19mm).

4 Functional Block Diagram



Outline

5 Edition History

Date	Version	Contents Updated
2026.3	Rev 1.0 Eng	Preliminary Draft

6 Pin Configuration and Functions

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	AGND	AINP_TRIGX_A	AGND	AGND	AINP_1	AINN_1	AGND	AGND	RBIAS<0>_A	RBIAS<1>_A	AGND	AGND	RESET_LOGIC_A	JGND	SERDOUTA15_N	SERDOUTA15_P	SERDOUTA13_N	SERDOUTA13_P	SERDOUTA11_N	SERDOUTA11_P	SERDOUTA10_N	JGND	A
B	AINP_SYSREF_A	AINN_TRIGX_A	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	TSKEW_BG_A	DGND	JGND	SERDOUTA14_N	SERDOUTA14_P	SERDOUTA12_N	SERDOUTA12_P	JGND	SERDOUTA10_P	SERDOUTA9_N	B
C	AINN_SYSREF_A	AGND	AGND	BVNN08<0>_A	BVNN08<0>_A	AVDD18_BUF<0>_A	AVDD18_BUF<0>_A	AVDD18_BUF<0>_A	BVNN08<0>_A	AGND	AGND	NC	POWERDOWN_A	DGND	DGND	JGND	JGND	JGND	JGND	JGND	SERDOUTA8_N	SERDOUTA9_P	C
D	AGND	AGND	AGND	AVDD18_BIAS<0>_A	AVDD18_ADC<0>_A	AGND	AGND	AVDD18_ADC<0>_A	BVNN08<0>_A	AGND	AGND	SCLK_A	GPIO<4>_A	DVDD09_A	DGND	DGND	JGND	DJVDD_A	DJVDD_A	JGND	SERDOUTA8_P	SERDOUTA7_N	D
E	AINP_CK_A	AGND	AGND	AVDD18_REF<0>_A	AVDD18_ADC<0>_A	AGND	AGND	AVDD18_ADC<0>_A	AGND	AGND	DGND	SDI_A	GPIO<3>_A	DVDD09_A	DVDD09_A	DGND	JGND	DJVDD_A	DJVDD_A	JGND	SERDOUTA6_N	SERDOUTA7_P	E
F	AINN_CK_A	AGND	AGND	AVDD18_CK<1>_A	AVDD18_ADC<0>_A	AGND	AGND	AVDD18_ADC<0>_A	TDIODE_N_A	AGND	RESET_ANALOGA	SDO_A	GPIO<2>_A	DVDD09_A	DVDD09_A	DGND	JGND	JGND	JGND	JGND	SERDOUTA6_P	SERDOUTA5_N	F
G	AGND	AGND	AGND	AVDD18_CK<0>_A	AVDD18_ADC<1>_A	AGND	AGND	AVDD18_ADC<1>_A	TDIODE_P_A	AGND	DGND	SPI_CSH_A	GPIO<1>_A	DVDD09_A	DVDD09_A	DGND	JGND	JVDD09_A	JVDD09_A	JGND	SERDOUTA4_N	SERDOUTA5_P	G
H	AGND	AGND	AGND	AVDD18_REF<1>_A	AVDD18_ADC<1>_A	AGND	AGND	AVDD18_ADC<1>_A	AGND	AGND	DGND	SYNCB_A	GPIO<0>_A	DVDD09_A	DVDD09_A	DGND	JGND	JVDD09_A	JVDD09_A	JGND	SERDOUTA4_P	SERDOUTA3_N	H
J	AINP_2	AGND	AGND	AVDD18_BIAS<1>_A	AVDD18_ADC<1>_A	AGND	AGND	AVDD18_ADC<1>_A	BVNN08<1>_A	AGND	DGND	FD<0>_A	FD<1>_A	DVDD09_A	DVDD09_A	DGND	JGND	JVDD09_A	JVDD09_A	JGND	SERDOUTA2_N	SERDOUTA3_P	J
K	AINN_2	AGND	AGND	BVNN08<1>_A	BVNN08<1>_A	AVDD18_BUF<1>_A	AVDD18_BUF<1>_A	AVDD18_BUF<1>_A	BVNN08<1>_A	AGND	DGND	NC	NC	DVDD09_A	DGND	DGND	JGND	JVDD09_A	JGND	JGND	SERDOUTA2_P	SERDOUTA1_N	K
L	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	DGND	DVDD18_A	DGND	DGND	DGND	JVDD18_A	JGND	SERDOUTA0_N	SERDOUTA0_P	JGND	SERDOUTA1_P	L
M	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	DGND	DVDD18_B	DGND	DGND	DGND	JVDD18_B	JGND	SERDOUTB15_N	SERDOUTB15_P	JGND	SERDOUTB14_P	M
N	AINN_3	AGND	AGND	BVNN08<0>_B	BVNN08<0>_B	AVDD18_BUF<0>_B	AVDD18_BUF<0>_B	AVDD18_BUF<0>_B	BVNN08<0>_B	AGND	DGND	NC	NC	DVDD09_B	DGND	DGND	JGND	JVDD09_B	JGND	JGND	SERDOUTB13_P	SERDOUTB14_N	N
P	AINP_3	AGND	AGND	AVDD18_BIAS<0>_B	AVDD18_ADC<0>_B	AGND	AGND	AVDD18_ADC<0>_B	BVNN08<0>_B	AGND	DGND	FD<0>_B	FD<1>_B	DVDD09_B	DVDD09_B	DGND	JGND	JVDD09_B	JVDD09_B	JGND	SERDOUTB13_N	SERDOUTB12_P	P
R	AGND	AGND	AGND	AVDD18_REF<0>_B	AVDD18_ADC<0>_B	AGND	AGND	AVDD18_ADC<0>_B	AGND	AGND	DGND	SYNCB_B	GPIO<0>_B	DVDD09_B	DVDD09_B	DGND	JGND	JVDD09_B	JVDD09_B	JGND	SERDOUTB11_P	SERDOUTB12_N	R
T	AGND	AGND	AGND	AVDD18_CK<1>_B	AVDD18_ADC<0>_B	AGND	AGND	AVDD18_ADC<0>_B	TDIODE_N_B	AGND	DGND	SPI_CSH_B	GPIO<1>_B	DVDD09_B	DVDD09_B	DGND	JGND	JVDD09_B	JVDD09_B	JGND	SERDOUTB11_N	SERDOUTB10_P	T
U	AINP_CK_B	AGND	AGND	AVDD18_CK<0>_B	AVDD18_ADC<1>_B	AGND	AGND	AVDD18_ADC<1>_B	TDIODE_P_B	AGND	RESET_ANALOGB	SDO_B	GPIO<2>_B	DVDD09_B	DVDD09_B	DGND	JGND	JGND	JGND	JGND	SERDOUTB9_P	SERDOUTB10_N	U
V	AINN_CK_B	AGND	AGND	AVDD18_REF<1>_B	AVDD18_ADC<1>_B	AGND	AGND	AVDD18_ADC<1>_B	AGND	AGND	DGND	SDI_B	GPIO<3>_B	DVDD09_B	DVDD09_B	DGND	JGND	DJVDD_B	DJVDD_B	JGND	SERDOUTB9_N	SERDOUTB8_P	V
W	AGND	AGND	AGND	AVDD18_BIAS<1>_B	AVDD18_ADC<1>_B	AGND	AGND	AVDD18_ADC<1>_B	BVNN08<1>_B	AGND	AGND	SCLK_B	GPIO<4>_B	DVDD09_B	DGND	DGND	JGND	DJVDD_B	DJVDD_B	JGND	SERDOUTB7_P	SERDOUTB8_N	W
Y	AINP_SYSREF_B	AGND	AGND	BVNN08<1>_B	BVNN08<1>_B	AVDD18_BUF<1>_B	AVDD18_BUF<1>_B	AVDD18_BUF<1>_B	BVNN08<1>_B	AGND	AGND	NC	POWERDOWN_B	DGND	DGND	JGND	JGND	JGND	JGND	JGND	SERDOUTB7_N	SERDOUTB6_P	Y
AA	AINN_SYSREF_B	AINP_TRIGX_B	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	TSKEW_BG_B	DGND	JGND	SERDOUTB1_N	SERDOUTB1_P	SERDOUTB3_N	SERDOUTB3_P	JGND	SERDOUTB5_P	SERDOUTB6_N	AA
AB	AGND	AINN_TRIGX_B	AGND	AGND	AINP_4	AINN_4	AGND	AGND	RBIAS<0>_B	RBIAS<1>_B	AGND	AGND	RESET_LOGIC_B	JGND	SERDOUTB0_N	SERDOUTB0_P	SERDOUTB2_N	SERDOUTB2_P	SERDOUTB4_N	SERDOUTB4_P	SERDOUTB5_N	JGND	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Top View Not to scale

Fig 6-1. 484-Ball Flip Chip BGA

Table 6-1. Pin Functions

TBD

7 Specifications

7.1 Electrical Characteristics

7.1.1 CAE2200s Specifications

Parameter	Conditions	CAE2200s			Unit
		Min	Typ	Max	
Analog Input					
Full-scale input range	Fully differential	0.5	0.8	1.0	Vpp,diff
Input Termination	Single-ended to AGND		50		Ω
	Differential		100		Ω
Single Input capacitance	Single-ended to AGND		400		fF
Differential Input capacitance	Differential inputs		80		fF
Input Common Mode	$V_{CM,input}$	0.40	0.45	0.50	V
Input Signal Bandwidth	-3dB bandwidth		TBD		GHz
SerDes Output					
Differential Output Voltage	Normal mode	0.45		0.50	Vpp,diff
Output Common Mode Voltage	AC coupled	0.57	0.63	0.79	V
Output Termination	Differential		100		Ω
Clock Input					
Differential Input Voltage	100 ohm differential, on-chip	0.3	1	2	Vpp,diff
Input Common Mode Voltage	$V_{CM,CLKIN}$	0.2	0.3	0.4	V
Clock Frequency	F_{CLK}			5.2	GHz
Duty Cycle			50.0		%
Single Input Capacitance	Single-ended to AGND		400		fF
Differential Input Capacitance	Differential inputs		80		fF
SYSREF Input					
Differential Input Voltage	100 ohm differential, on-chip	0.5	1.0	2.0	Vpp,diff
Input Common Mode Voltage	$V_{CM,SYSREFIN}$		0.9		V
Frequency	Periodic mode		32.5	81.25	MHz
Pulse Width	Burst and Periodic modes	192.31			ps
Single Input Capacitance	Single-ended to AGND		450		fF
Differential Input Capacitance	Differential inputs		90		fF
Reference Voltage					
Internal Reference Voltage	Fully Differential	±0.39	±0.4	±0.41	V
Tempco	From -40°C to 125°C		±50	±100	ppm/°C
DC Accuracy					
Resolution	DC code		12		bit
INL	Best-Fit		±2.7		LSB
DNL	(no missing code)		±0.6		LSB
Offset Error	DC code error		±3		mV
Code Error Rate	Whole chip		$< 10^{-15}$		Error/ samples

CAE2200s Specifications (Continued)

Parameter	Conditions *Single-Channel Mode , 20.8 GSPS*	CAE2200s			Unit
		Min	Typ	Max	
AC Accuracy					
SNR	Fin = 1GHz, -1.0 dBFS (0.8Vpp FS)		47.6		dBFS
	Fin = 1GHz, -10.0 dBFS (0.8Vpp FS)		49.4		
	Fin = 2GHz, -1.0 dBFS (0.8Vpp FS)		46.3		dBFS
	Fin = 2GHz, -10.0 dBFS (0.8Vpp FS)		49.0		
	Fin = 3GHz, -1.0 dBFS (0.8Vpp FS)		45.1		dBFS
	Fin = 3GHz, -10.0 dBFS (0.8Vpp FS)		48.3		
	Fin = 4GHz, -1.0 dBFS (0.8Vpp FS)		43.8		dBFS
	Fin = 4GHz, -10.0 dBFS (0.8Vpp FS)		48.0		
	Fin = 5GHz, -1.0 dBFS (0.8Vpp FS)		43.6		dBFS
	Fin = 5GHz, -10.0 dBFS (0.8Vpp FS)		47.7		
SINAD	Fin = 1GHz, -1.0 dBFS (0.8Vpp FS)		47.5		dBFS
	Fin = 1GHz, -10.0 dBFS (0.8Vpp FS)		49.2		
	Fin = 2GHz, -1.0 dBFS (0.8Vpp FS)		46.2		dBFS
	Fin = 2GHz, -10.0 dBFS (0.8Vpp FS)		48.8		
	Fin = 3GHz, -1.0 dBFS (0.8Vpp FS)		45.0		dBFS
	Fin = 3GHz, -10.0 dBFS (0.8Vpp FS)		48.0		
	Fin = 4GHz, -1.0 dBFS (0.8Vpp FS)		43.6		dBFS
	Fin = 4GHz, -10.0 dBFS (0.8Vpp FS)		47.8		
	Fin = 5GHz, -1.0 dBFS (0.8Vpp FS)		43.4		dBFS
	Fin = 5GHz, -10.0 dBFS (0.8Vpp FS)		47.4		
SFDR	Fin = 1GHz, -1.0 dBFS (0.8Vpp FS)		63.8		dBc
	Fin = 1GHz, -10.0 dBFS (0.8Vpp FS)		68.7		
	Fin = 2GHz, -1.0 dBFS (0.8Vpp FS)		64.8		dBc
	Fin = 2GHz, -10.0 dBFS (0.8Vpp FS)		66.9		
	Fin = 3GHz, -1.0 dBFS (0.8Vpp FS)		65.6		dBc
	Fin = 3GHz, -10.0 dBFS (0.8Vpp FS)		67.4		
	Fin = 4GHz, -1.0 dBFS (0.8Vpp FS)		61.5		dBc
	Fin = 4GHz, -10.0 dBFS (0.8Vpp FS)		68.5		
	Fin = 5GHz, -1.0 dBFS (0.8Vpp FS)		58.7		dBc
	Fin = 5GHz, -10.0 dBFS (0.8Vpp FS)		66.6		

CAE2200s Specifications (Continued)

Parameter	Conditions *Single-Channel Mode , 20.8 GSPS*	CAE2200s			Unit
		Min	Typ	Max	
AC Accuracy					
HD2	Fin = 1GHz, -1.0 dBFS (0.8Vpp FS)		-88.5		dBFS
	Fin = 1GHz, -10.0 dBFS (0.8Vpp FS)		-73.0		
	Fin = 2GHz, -1.0 dBFS (0.8Vpp FS)		-74.4		dBFS
	Fin = 2GHz, -10.0 dBFS (0.8Vpp FS)		-74.9		
	Fin = 3GHz, -1.0 dBFS (0.8Vpp FS)		-74.5		dBFS
	Fin = 3GHz, -10.0 dBFS (0.8Vpp FS)		-78.7		
	Fin = 4GHz, -1.0 dBFS (0.8Vpp FS)		-70.0		dBFS
	Fin = 4GHz, -10.0 dBFS (0.8Vpp FS)		-75.3		
	Fin = 5GHz, -1.0 dBFS (0.8Vpp FS)		-71.1		dBFS
	Fin = 5GHz, -10.0 dBFS (0.8Vpp FS)		-68.8		
HD3	Fin = 1GHz, -1.0 dBFS (0.8Vpp FS)		-64.0		dBFS
	Fin = 1GHz, -10.0 dBFS (0.8Vpp FS)		-77.5		
	Fin = 2GHz, -1.0 dBFS (0.8Vpp FS)		-65.0		dBFS
	Fin = 2GHz, -10.0 dBFS (0.8Vpp FS)		-78.9		
	Fin = 3GHz, -1.0 dBFS (0.8Vpp FS)		-65.6		dBFS
	Fin = 3GHz, -10.0 dBFS (0.8Vpp FS)		-67.4		
	Fin = 4GHz, -1.0 dBFS (0.8Vpp FS)		-61.9		dBFS
	Fin = 4GHz, -10.0 dBFS (0.8Vpp FS)		-74.6		
	Fin = 5GHz, -1.0 dBFS (0.8Vpp FS)		-58.9		dBFS
	Fin = 5GHz, -10.0 dBFS (0.8Vpp FS)		-70.6		
ENOB	Fin = 1GHz, -1.0 dBFS (0.8Vpp FS)		7.6		Bit
	Fin = 1GHz, -10.0 dBFS (0.8Vpp FS)		7.9		
	Fin = 2GHz, -1.0 dBFS (0.8Vpp FS)		7.4		Bit
	Fin = 2GHz, -10.0 dBFS (0.8Vpp FS)		7.8		
	Fin = 3GHz, -1.0 dBFS (0.8Vpp FS)		7.2		Bit
	Fin = 3GHz, -10.0 dBFS (0.8Vpp FS)		7.7		
	Fin = 4GHz, -1.0 dBFS (0.8Vpp FS)		7.0		Bit
	Fin = 4GHz, -10.0 dBFS (0.8Vpp FS)		7.6		
	Fin = 5GHz, -1.0 dBFS (0.8Vpp FS)		6.9		Bit
	Fin = 5GHz, -10.0 dBFS (0.8Vpp FS)		7.6		

CAE2200s Specifications (Continued)

Parameter	Conditions	CAE2200s			Unit
		Min	Typ	Max	
AC Accuracy					
Noise Floor Density	At 1GHz, -10 dBFS (0.8Vpp FS)		-149.5		dBFS/√Hz
Speed					
ADC Sampling rate	Single-channel		20.8		GSPS
	Dual-Channel		10.4		GSPS
JESD204B lane rate	SerDes lane rate, 100 ohm termination	1.25	13.0		Gbps
Power Supplies					
AVDD18_BUF , AVDD18_ADC , AVDD18_BIAS , AVDD18_REF , AVDD18_CK , DVDD18 , JVDD18	1.8V power supplies	1.7	1.8	1.9	V
DVDD09 , JVDD09 , DJVDD	0.95V power supplies	0.9	0.95	0.975	V
BVNN08	Analog negative power supplies	-0.95	-1.0	-1.05	V
Current (1.8V supplies)	Normal mode, all background calibrations enable & DDC off (single)		2500		mA
	Normal mode, all background calibrations enable & DDC off (dual)		2700		
Current (0.95V supplies)	Normal mode, all background calibrations enable & DDC off		1480		mA
Current (1.8V supplies)	Power down		52		mA
Current (0.95V supplies)	Power down		20		mA
Power Consumption	Normal mode, all background calibrations enable & DDC off (single)		6.0		W
	Normal mode, all background calibrations enable & DDC off (dual)		6.34		
Junction Temperature	T_{MIN} to T_{MAX}	-40		115	°C
Long-Term Reliability	For Pro-longed use	-40		105	°C

7.1.2 CAE2300s Specifications

Parameter	Conditions	CAE2300s			Unit
		Min	Typ	Max	
Analog Input					
Full-scale input range	Fully differential	0.5	0.8	1.0	Vpp,diff
Input Termination	Single-ended to AGND		50		Ω
	Differential		100		Ω
Single Input capacitance	Single-ended to AGND		400		fF
Differential Input capacitance	Differential inputs		80		fF
Input Common Mode	$V_{CM,input}$	0.40	0.45	0.50	V
Input Signal Bandwidth	-3dB bandwidth		TBD		GHz
SerDes Output					
Differential Output Voltage	Normal mode	0.45		0.50	Vpp,diff
Output Common Mode Voltage	AC coupled	0.57	0.63	0.79	V
Output Termination	Differential		100		Ω
Clock Input					
Differential Input Voltage	100 ohm differential, on-chip	0.3	1	2	Vpp,diff
Input Common Mode Voltage	$V_{CM,CLKIN}$	0.2	0.3	0.4	V
Clock Frequency	F_{CLK}			4.0	GHz
Duty Cycle			50.0		%
Single Input Capacitance	Single-ended to AGND		400		fF
Differential Input Capacitance	Differential inputs		80		fF
SYSREF Input					
Differential Input Voltage	100 ohm differential, on-chip	0.5	1.0	2.0	Vpp,diff
Input Common Mode Voltage	$V_{CM,SYSREFIN}$		0.9		V
Frequency	Periodic mode		25	62.5	MHz
Pulse Width	Burst and Periodic modes	250			ps
Single Input Capacitance	Single-ended to AGND		450		fF
Differential Input Capacitance	Differential inputs		90		fF
Reference Voltage					
Internal Reference Voltage	Fully Differential	±0.39	±0.4	±0.41	V
Tempco	From -40°C to 125°C		±50	±100	ppm/°C
DC Accuracy					
Resolution	DC code		12		bit
INL	Best-Fit		±1.5		LSB
DNL	(no missing code)		±0.67		LSB
Offset Error	DC code error		±3		mV
Code Error Rate	Whole chip		$< 10^{-15}$		Error/ samples

CAE2300s Specifications (Continued)

Parameter	Conditions *Single-Channel Mode , 15.2 GSPS*	CAE2300s			Unit
		Min	Typ	Max	
AC Accuracy					
SNR	Fin = 1GHz, -1.0 dBFS (0.8Vpp FS)		50.2		dBFS
	Fin = 1GHz, -10.0 dBFS (0.8Vpp FS)		51.1		
	Fin = 2GHz, -1.0 dBFS (0.8Vpp FS)		48.6		dBFS
	Fin = 2GHz, -10.0 dBFS (0.8Vpp FS)		50.7		
	Fin = 3GHz, -1.0 dBFS (0.8Vpp FS)		47.3		dBFS
	Fin = 3GHz, -10.0 dBFS (0.8Vpp FS)		50.5		
	Fin = 4GHz, -1.0 dBFS (0.8Vpp FS)		46.0		dBFS
	Fin = 4GHz, -10.0 dBFS (0.8Vpp FS)		50.1		
	Fin = 5GHz, -1.0 dBFS (0.8Vpp FS)		45.1		dBFS
	Fin = 5GHz, -10.0 dBFS (0.8Vpp FS)		49.4		
SINAD	Fin = 1GHz, -1.0 dBFS (0.8Vpp FS)		50.0		dBFS
	Fin = 1GHz, -10.0 dBFS (0.8Vpp FS)		51.0		
	Fin = 2GHz, -1.0 dBFS (0.8Vpp FS)		48.6		dBFS
	Fin = 2GHz, -10.0 dBFS (0.8Vpp FS)		50.7		
	Fin = 3GHz, -1.0 dBFS (0.8Vpp FS)		47.3		dBFS
	Fin = 3GHz, -10.0 dBFS (0.8Vpp FS)		50.5		
	Fin = 4GHz, -1.0 dBFS (0.8Vpp FS)		45.9		dBFS
	Fin = 4GHz, -10.0 dBFS (0.8Vpp FS)		50.1		
	Fin = 5GHz, -1.0 dBFS (0.8Vpp FS)		44.9		dBFS
	Fin = 5GHz, -10.0 dBFS (0.8Vpp FS)		49.3		
SFDR	Fin = 1GHz, -1.0 dBFS (0.8Vpp FS)		66.9		dBc
	Fin = 1GHz, -10.0 dBFS (0.8Vpp FS)		70.6		
	Fin = 2GHz, -1.0 dBFS (0.8Vpp FS)		65.8		dBc
	Fin = 2GHz, -10.0 dBFS (0.8Vpp FS)		69.4		
	Fin = 3GHz, -1.0 dBFS (0.8Vpp FS)		64.4		dBc
	Fin = 3GHz, -10.0 dBFS (0.8Vpp FS)		66.5		
	Fin = 4GHz, -1.0 dBFS (0.8Vpp FS)		61.5		dBc
	Fin = 4GHz, -10.0 dBFS (0.8Vpp FS)		68.8		
	Fin = 5GHz, -1.0 dBFS (0.8Vpp FS)		61.1		dBc
	Fin = 5GHz, -10.0 dBFS (0.8Vpp FS)		67.7		

CAE2300s Specifications (Continued)

Parameter	Conditions *Single-Channel Mode , 15.2 GSPS*	CAE2300s			Unit
		Min	Typ	Max	
AC Accuracy					
HD2	Fin = 1GHz, -1.0 dBFS (0.8Vpp FS)		-80.0		dBFS
	Fin = 1GHz, -10.0 dBFS (0.8Vpp FS)		-84.4		
	Fin = 2GHz, -1.0 dBFS (0.8Vpp FS)		-81.4		dBFS
	Fin = 2GHz, -10.0 dBFS (0.8Vpp FS)		-76.4		
	Fin = 3GHz, -1.0 dBFS (0.8Vpp FS)		-70.2		dBFS
	Fin = 3GHz, -10.0 dBFS (0.8Vpp FS)		-79.1		
	Fin = 4GHz, -1.0 dBFS (0.8Vpp FS)		-72.9		dBFS
	Fin = 4GHz, -10.0 dBFS (0.8Vpp FS)		-85.7		
	Fin = 5GHz, -1.0 dBFS (0.8Vpp FS)		-64.7		dBFS
	Fin = 5GHz, -10.0 dBFS (0.8Vpp FS)		-71.8		
HD3	Fin = 1GHz, -1.0 dBFS (0.8Vpp FS)		-67.1		dBFS
	Fin = 1GHz, -10.0 dBFS (0.8Vpp FS)		-87.1		
	Fin = 2GHz, -1.0 dBFS (0.8Vpp FS)		-74.0		dBFS
	Fin = 2GHz, -10.0 dBFS (0.8Vpp FS)		-75.4		
	Fin = 3GHz, -1.0 dBFS (0.8Vpp FS)		-74.4		dBFS
	Fin = 3GHz, -10.0 dBFS (0.8Vpp FS)		-81.3		
	Fin = 4GHz, -1.0 dBFS (0.8Vpp FS)		-71.6		dBFS
	Fin = 4GHz, -10.0 dBFS (0.8Vpp FS)		-72.7		
	Fin = 5GHz, -1.0 dBFS (0.8Vpp FS)		-61.6		dBFS
	Fin = 5GHz, -10.0 dBFS (0.8Vpp FS)		-68.0		
ENOB	Fin = 1GHz, -1.0 dBFS (0.8Vpp FS)		8.0		Bit
	Fin = 1GHz, -10.0 dBFS (0.8Vpp FS)		8.2		
	Fin = 2GHz, -1.0 dBFS (0.8Vpp FS)		7.8		Bit
	Fin = 2GHz, -10.0 dBFS (0.8Vpp FS)		8.1		
	Fin = 3GHz, -1.0 dBFS (0.8Vpp FS)		7.6		Bit
	Fin = 3GHz, -10.0 dBFS (0.8Vpp FS)		8.1		
	Fin = 4GHz, -1.0 dBFS (0.8Vpp FS)		7.3		Bit
	Fin = 4GHz, -10.0 dBFS (0.8Vpp FS)		8.0		
	Fin = 5GHz, -1.0 dBFS (0.8Vpp FS)		7.2		Bit
	Fin = 5GHz, -10.0 dBFS (0.8Vpp FS)		7.9		

CAE2300s Specifications (Continued)

Parameter	Conditions	CAE2300s			Unit
		Min	Typ	Max	
AC Accuracy					
Noise Floor Density	At 1GHz, -10 dBFS (0.8Vpp FS)		-149.9		dBFS/√Hz
Speed					
ADC Sampling rate	Single-channel		15.2		GSPS
	Dual-Channel		7.6		GSPS
JESD204B lane rate	SerDes lane rate, 100 ohm termination	1.25	10.0		Gbps
Power Supplies					
AVDD18_BUF , AVDD18_ADC , AVDD18_BIAS , AVDD18_REF , AVDD18_CK , DVDD18 , JVDD18	1.8V power supplies	1.7	1.8	1.9	V
DVDD09 , JVDD09 , DJVDD	0.95V power supplies	0.9	0.95	0.975	V
BVNN08	Analog negative power supplies	-0.95	-1.0	-1.05	V
Current (1.8V supplies)	Normal mode, all background calibrations enable & DDC off (single)		2220		mA
	Normal mode, all background calibrations enable & DDC off (dual)		2420		
Current (0.95V supplies)	Normal mode, all background calibrations enable & DDC off		1320		mA
Current (1.8V supplies)	Power down		52		mA
Current (0.95V supplies)	Power down		20		mA
Power Consumption	Normal mode, all background calibrations enable & DDC off (single)		5.3		W
	Normal mode, all background calibrations enable && DDC off (dual)		5.62		
Junction Temperature	T_{MIN} to T_{MAX}	-40		115	°C
Long-Term Reliability	For Pro-longed use	-40		105	°C

7.1.3 CAE2400s Specifications

Parameter	Conditions	CAE2400s			Unit
		Min	Typ	Max	
Analog Input					
Full-scale input range	Fully differential	0.5	0.8	1.0	Vpp,diff
Input Termination	Single-ended to AGND		50		Ω
	Differential		100		Ω
Single Input capacitance	Single-ended to AGND		400		fF
Differential Input capacitance	Differential inputs		80		fF
Input Common Mode	$V_{CM,input}$	0.40	0.45	0.50	V
Input Signal Bandwidth	-3dB bandwidth		TBD		GHz
SerDes Output					
Differential Output Voltage	Normal mode	0.45		0.50	Vpp,diff
Output Common Mode Voltage	AC coupled	0.57	0.63	0.79	V
Output Termination	Differential		100		Ω
Clock Input					
Differential Input Voltage	100 ohm differential, on-chip	0.3	1	2	Vpp,diff
Input Common Mode Voltage	$V_{CM,CLKIN}$	0.2	0.3	0.4	V
Clock Frequency	F_{CLK}			3.0	GHz
Duty Cycle			50.0		%
Single Input Capacitance	Single-ended to AGND		400		fF
Differential Input Capacitance	Differential inputs		80		fF
SYSREF Input					
Differential Input Voltage	100 ohm differential, on-chip	0.5	1.0	2.0	Vpp,diff
Input Common Mode Voltage	$V_{CM,SYSREFIN}$		0.9		V
Frequency	Periodic mode		18.75	46.875	MHz
Pulse Width	Burst and Periodic modes	333.33			ps
Single Input Capacitance	Single-ended to AGND		450		fF
Differential Input Capacitance	Differential inputs		90		fF
Reference Voltage					
Internal Reference Voltage	Fully Differential	±0.39	±0.4	±0.41	V
Tempco	From -40°C to 125°C		±50	±100	ppm/°C
DC Accuracy					
Resolution	DC code		12		bit
INL	Best-Fit		±1.8		LSB
DNL	(no missing code)		±0.63		LSB
Offset Error	DC code error		±3		mV
Code Error Rate	Whole chip		$< 10^{-15}$		Error/ samples

CAE2400s Specifications (Continued)

Parameter	Conditions *Single-Channel Mode , 12 GSPS*	CAE2400s			Unit
		Min	Typ	Max	
AC Accuracy					
SNR	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		50.8		dBFS
	Fin = 1.09GHz, -10.0 dBFS (0.8Vpp FS)		51.5		
	Fin = 1.9GHz, -1.0 dBFS (0.8Vpp FS)		49.6		dBFS
	Fin = 1.9GHz, -10.0 dBFS (0.8Vpp FS)		51.2		
	Fin = 2.9GHz, -1.0 dBFS (0.8Vpp FS)		47.9		dBFS
	Fin = 2.9GHz, -10.0 dBFS (0.8Vpp FS)		51.2		
	Fin = 3.9GHz, -1.0 dBFS (0.8Vpp FS)		46.1		dBFS
	Fin = 3.9GHz, -10.0 dBFS (0.8Vpp FS)		50.7		
	Fin = 4.9GHz, -1.0 dBFS (0.8Vpp FS)		45.7		dBFS
	Fin = 4.9GHz, -10.0 dBFS (0.8Vpp FS)		49.8		
SINAD	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		50.6		dBFS
	Fin = 1.09GHz, -10.0 dBFS (0.8Vpp FS)		51.3		
	Fin = 1.9GHz, -1.0 dBFS (0.8Vpp FS)		49.4		dBFS
	Fin = 1.9GHz, -10.0 dBFS (0.8Vpp FS)		51.1		
	Fin = 2.9GHz, -1.0 dBFS (0.8Vpp FS)		47.8		dBFS
	Fin = 2.9GHz, -10.0 dBFS (0.8Vpp FS)		51.0		
	Fin = 3.9GHz, -1.0 dBFS (0.8Vpp FS)		45.9		dBFS
	Fin = 3.9GHz, -10.0 dBFS (0.8Vpp FS)		50.6		
	Fin = 4.9GHz, -1.0 dBFS (0.8Vpp FS)		45.6		dBFS
	Fin = 4.9GHz, -10.0 dBFS (0.8Vpp FS)		49.7		
SFDR	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		68.7		dBc
	Fin = 1.09GHz, -10.0 dBFS (0.8Vpp FS)		65.6		
	Fin = 1.9GHz, -1.0 dBFS (0.8Vpp FS)		66.3		dBc
	Fin = 1.9GHz, -10.0 dBFS (0.8Vpp FS)		68.3		
	Fin = 2.9GHz, -1.0 dBFS (0.8Vpp FS)		64.1		dBc
	Fin = 2.9GHz, -10.0 dBFS (0.8Vpp FS)		69.4		
	Fin = 3.9GHz, -1.0 dBFS (0.8Vpp FS)		61.5		dBc
	Fin = 3.9GHz, -10.0 dBFS (0.8Vpp FS)		61.9		
	Fin = 4.9GHz, -1.0 dBFS (0.8Vpp FS)		61.3		dBc
	Fin = 4.9GHz, -10.0 dBFS (0.8Vpp FS)		67.2		

CAE2400s Specifications (Continued)

Parameter	Conditions *Single-Channel Mode , 12 GSPS*	CAE2400s			Unit
		Min	Typ	Max	
AC Accuracy					
HD2	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		-78.4		dBFS
	Fin = 1.09GHz, -10.0 dBFS (0.8Vpp FS)		-90.5		
	Fin = 1.9GHz, -1.0 dBFS (0.8Vpp FS)		-75.2		dBFS
	Fin = 1.9GHz, -10.0 dBFS (0.8Vpp FS)		-99.2		
	Fin = 2.9GHz, -1.0 dBFS (0.8Vpp FS)		-76.1		dBFS
	Fin = 2.9GHz, -10.0 dBFS (0.8Vpp FS)		-80.9		
	Fin = 3.9GHz, -1.0 dBFS (0.8Vpp FS)		-68.0		dBFS
	Fin = 3.9GHz, -10.0 dBFS (0.8Vpp FS)		-79.9		
	Fin = 4.9GHz, -1.0 dBFS (0.8Vpp FS)		-68.0		dBFS
	Fin = 4.9GHz, -10.0 dBFS (0.8Vpp FS)		-93.8		
HD3	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		-71.0		dBFS
	Fin = 1.09GHz, -10.0 dBFS (0.8Vpp FS)		-65.6		
	Fin = 1.9GHz, -1.0 dBFS (0.8Vpp FS)		-70.0		dBFS
	Fin = 1.9GHz, -10.0 dBFS (0.8Vpp FS)		-69.2		
	Fin = 2.9GHz, -1.0 dBFS (0.8Vpp FS)		-69.0		dBFS
	Fin = 2.9GHz, -10.0 dBFS (0.8Vpp FS)		-69.7		
	Fin = 3.9GHz, -1.0 dBFS (0.8Vpp FS)		-66.4		dBFS
	Fin = 3.9GHz, -10.0 dBFS (0.8Vpp FS)		-69.7		
	Fin = 4.9GHz, -1.0 dBFS (0.8Vpp FS)		-62.7		dBFS
	Fin = 4.9GHz, -10.0 dBFS (0.8Vpp FS)		-68.8		
ENOB	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		8.1		Bit
	Fin = 1.09GHz, -10.0 dBFS (0.8Vpp FS)		8.2		
	Fin = 1.9GHz, -1.0 dBFS (0.8Vpp FS)		7.9		Bit
	Fin = 1.9GHz, -10.0 dBFS (0.8Vpp FS)		8.2		
	Fin = 2.9GHz, -1.0 dBFS (0.8Vpp FS)		7.6		Bit
	Fin = 2.9GHz, -10.0 dBFS (0.8Vpp FS)		8.2		
	Fin = 3.9GHz, -1.0 dBFS (0.8Vpp FS)		7.3		Bit
	Fin = 3.9GHz, -10.0 dBFS (0.8Vpp FS)		8.1		
	Fin = 4.9GHz, -1.0 dBFS (0.8Vpp FS)		7.3		Bit
	Fin = 4.9GHz, -10.0 dBFS (0.8Vpp FS)		8.0		

CAE2400s Specifications (Continued)

Parameter	Conditions	CAE2400s			Unit
		Min	Typ	Max	
AC Accuracy					
Noise Floor Density	At 1.09GHz, -10 dBFS (0.8Vpp FS)		-149.3		dBFS/√Hz
Speed					
ADC Sampling rate	Single-channel		12.0		GSPS
	Dual-Channel		6.0		GSPS
JESD204B lane rate	SerDes lane rate, 100 ohm termination	1.25	7.5	15.0	Gbps
Power Supplies					
AVDD18_BUF , AVDD18_ADC , AVDD18_BIAS , AVDD18_REF , AVDD18_CK , DVDD18 , JVDD18	1.8V power supplies	1.7	1.8	1.9	V
DVDD09 , JVDD09 , DJVDD	0.95V power supplies	0.9	0.95	0.975	V
BVNN08	Analog negative power supplies	-0.95	-1.0	-1.05	V
Current (1.8V supplies)	Normal mode, all background calibrations enable & DDC off (single)		1940		mA
	Normal mode, all background calibrations enable & DDC off (dual)		2084		
Current (0.95V supplies)	Normal mode, all background calibrations enable & DDC off		1300		mA
Current (1.8V supplies)	Power down		52		mA
Current (0.95V supplies)	Power down		20		mA
Power Consumption	Normal mode, all background calibrations enable & DDC off (single)		4.72		W
	Normal mode, all background calibrations enable & DDC off (dual)		5.0		
Junction Temperature	T_{MIN} to T_{MAX}	-40		115	°C
Long-Term Reliability	For Pro-longed use	-40		105	°C

7.2 Timing Requirements

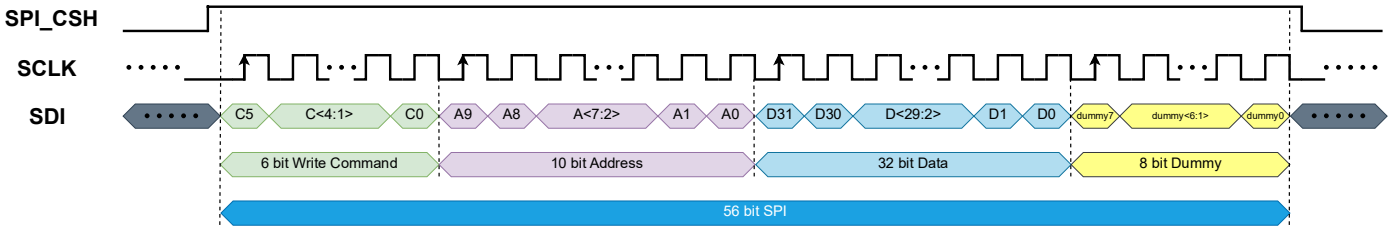


Fig 7-1. SPI Write Timing Diagram

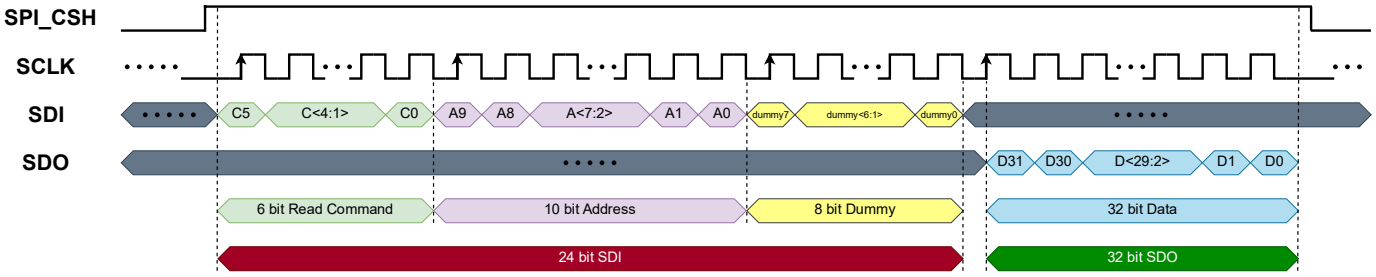


Fig 7-2. SPI Read Timing Diagram

The device features a standard 4-wire SPI interface for register configuration and JESD204B link control, supporting both internal SPI registers and JESD204B APB-mapped registers.

SPI_CSH (Chip Select) is an **active-high** signal:

- The device is selected (enabled for SPI transactions) when **SPI_CSH = 1** (logic high).
- The device is deselected (SPI interface disabled, outputs tri-stated where applicable) when **SPI_CSH = 0** (logic low).
- After chip reset (power-on reset or soft reset), **SPI_CSH** defaults to logic **1** (active / selected state by default). However, to ensure no unintended transactions occur post-reset, the master should drive **SPI_CSH** low during reset assertion and only bring it high when initiating a valid transfer.

Note: This active-high polarity is non-standard compared to the conventional active-low Chip Select used in most SPI peripherals. The master controller must configure its GPIO or SPI hardware accordingly (e.g., invert polarity if using a standard active-low driver).

All SPI transactions use a fixed **56-bit** frame format:

- Bits [55:50]: 6-bit command field (MSB first)
- Bits [49:40]: 10-bit address field
- Bits [39:0]: 40-bit data field

Command codes:

- 6'b0001_00 → Write register (SPI or APB)
- 6'b0010_00 → Read register (SPI or APB)

Address decoding:

- Addresses with MSB = 0 (0x_xxxx_xxxx) → Internal SPI configuration registers
- Addresses with MSB = 1 (1x_xxxx_xxxx) → JESD204B APB registers

SPI Write Transaction Example

Write to internal SPI register at address 10'h001 with data 32'h14183102:

- Command: 6'b0001_00
- Address: 10'b00_0000_0001
- Data: 32'h14183102 (byte order: 14 18 31 02)
- Padding: 8'b0000_0000 (dummy bits on SDI)

Timing sequence (56 SCLK cycles total):

1. First 6 SCLK: SDI = 000100 (write command)
2. Next 10 SCLK: SDI = 0000000001 (address 001h)
3. Next 32 SCLK: SDI = 00010100 00011000 00110001 00000010 (data)
4. Final 8 SCLK: SDI = 00000000 (dummy, ignored)

SPI_CSH must be held high (active) throughout the entire 56-bit transaction. After completion, the master may drive **SPI_CSH** low to deselect the device.

SPI Read Transaction Example

Read from internal SPI register at address 10'h000:

- Command: 6'b0010_00
- Address: 10'b00_0000_0000
- Dummy (TX): 8'b0000_0000 (turn-around)
- Dummy (RX padding): 32'b0...0 (SDI = 0 during readback)

Timing sequence:

1. First 6 SCLK: SDI = 001000 (read command)
2. Next 10 SCLK: SDI = 0000000000 (address 000h)
3. Next 8 SCLK: SDI = 00000000 (dummy cycles for device to prepare data)
4. Final 32 SCLK: SDI = all 0 (master dummy); device drives read data on **SDO**

SPI_CSH held high during the transaction.

Clocking and Edge Definitions

- Master changes SDI on **SCLK falling edge**
- Device samples SDI on **SCLK rising edge**
- Device updates SDO on **SCLK rising edge**
- Master samples SDO on **SCLK falling edge**

JESD204B APB Register Access

APB registers are accessed using the same 56-bit frame when address MSB = 1.

Example: APB Write to address 10'h204 with 8-bit data 8'h80:

- Command: 6'b0001_00
- Address: 10'b10_0000_0100
- Data[39:32]: 8'h80
- Data[31:0]: 32'h00000000 (dummy)

Example: APB Read from address 10'h204:

- Command: 6'b0010_00
- Address: 10'b10_0000_0100
- Dummy TX: 8'b00000000
- Read data: Returned in bits [39:32] on SDO (next 8 bits after dummy)
- Remaining: 24'b0...0 (dummy padding)

7.3 Typical Performance (AC coupled)

CAE2200s
(Single Channel Mode)

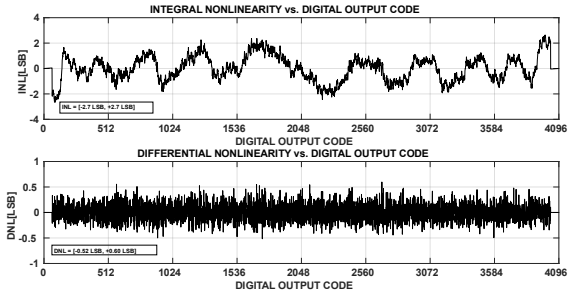


Fig 7-3. INL/DNL at Fin = 180MHz, 20.8GSPS (0.8Vpp FS)

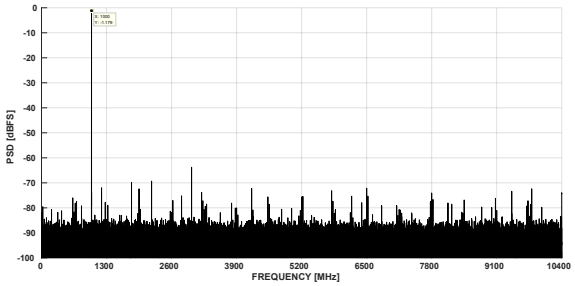


Fig 7-4. FFT at Fin = 1GHz, 20.8GSPS (0.8Vpp FS, -1dBFS)

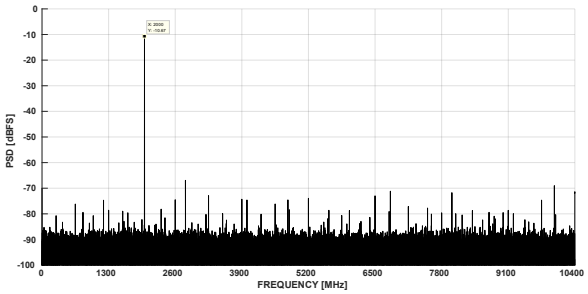


Fig 7-5. FFT at Fin = 2GHz, 20.8GSPS (0.8Vpp FS, -1dBFS)

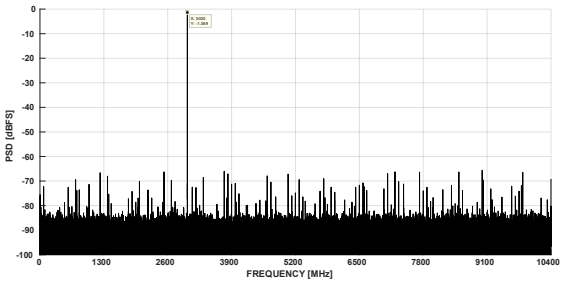


Fig 7-6. FFT at Fin = 3GHz, 20.8GSPS (0.8Vpp FS, -1dBFS)

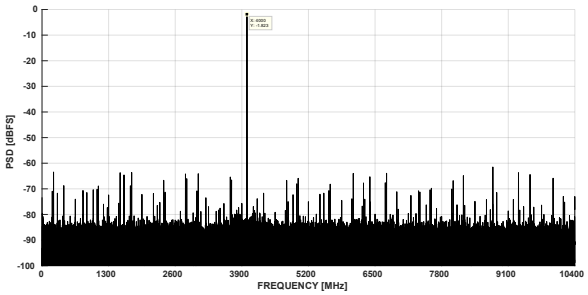


Fig 7-7. FFT at Fin = 4GHz, 20.8GSPS (0.8Vpp FS, -1dBFS)

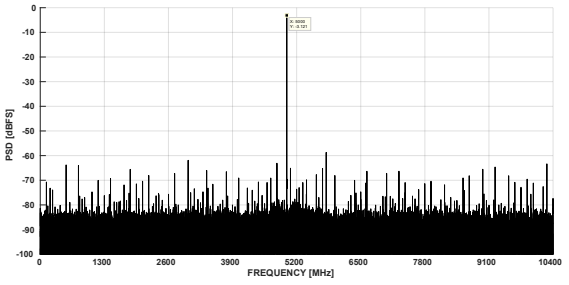


Fig 7-8. FFT at Fin = 5GHz, 20.8GSPS (0.8Vpp FS, -1dBFS)

CAE2200s
(Single Channel Mode)

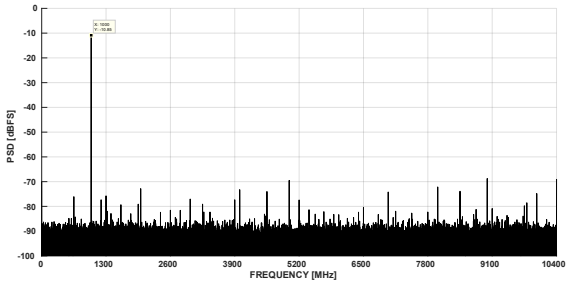


Fig 7-9. FFT at Fin = 1GHz, 20.8GSPS (0.8Vpp FS, -10dBFS)

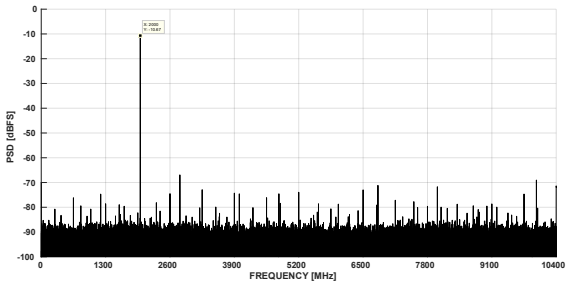


Fig 7-10. FFT at Fin = 2GHz, 20.8GSPS (0.8Vpp FS, -10dBFS)

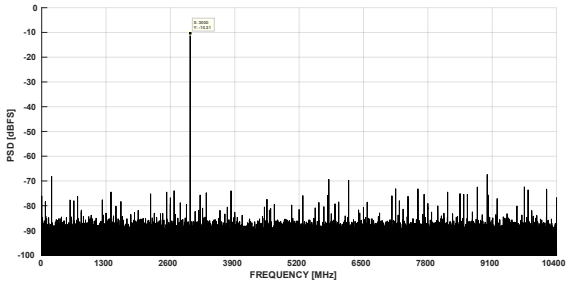


Fig 7-11. FFT at Fin = 3GHz, 20.8GSPS (0.8Vpp FS, -10dBFS)

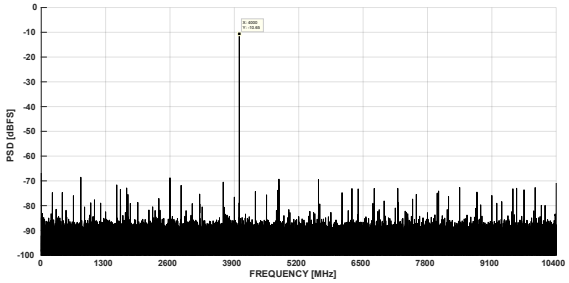


Fig 7-12. FFT at Fin = 4GHz, 20.8GSPS (0.8Vpp FS, -10dBFS)

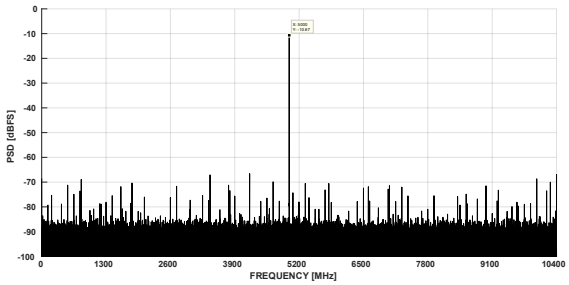


Fig 7-13. FFT at Fin = 5GHz, 20.8GSPS (0.8Vpp FS, -10dBFS)

CAE2300s
(Single Channel Mode)

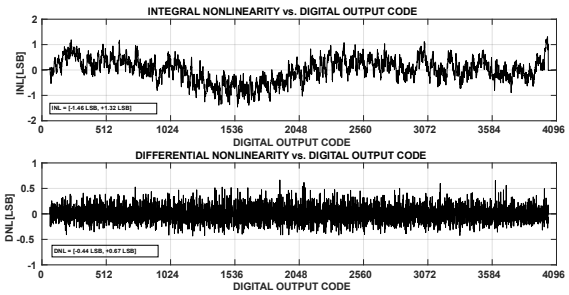


Fig 7-14. INL/DNL at Fin = 180MHz, 15.2GSPS (0.8Vpp FS)

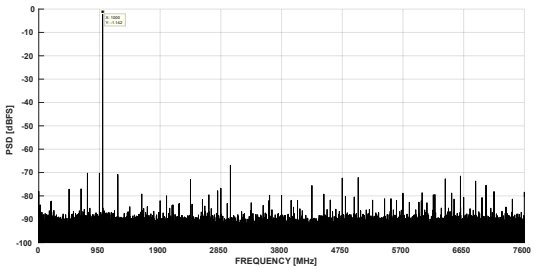


Fig 7-15. FFT at Fin = 1GHz, 15.2GSPS (0.8Vpp FS, -1dBFS)

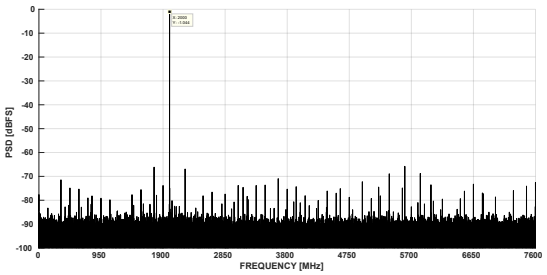


Fig 7-16. FFT at Fin = 2GHz, 15.2GSPS (0.8Vpp FS, -1dBFS)

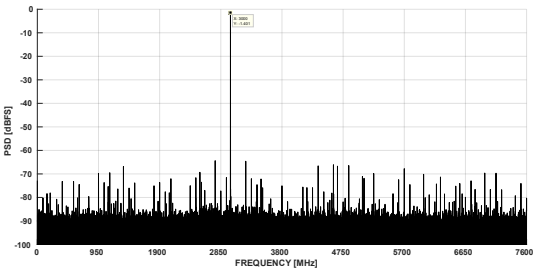


Fig 7-17. FFT at Fin = 3GHz, 15.2GSPS (0.8Vpp FS, -1dBFS)

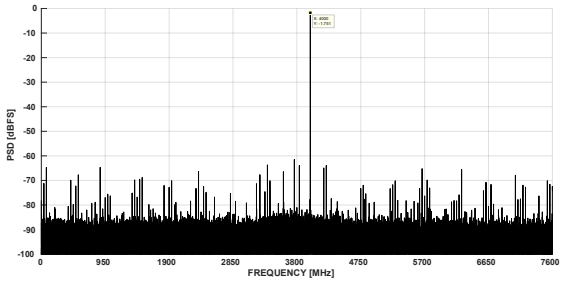


Fig 7-18. FFT at Fin = 4GHz, 15.2GSPS (0.8Vpp FS, -1dBFS)

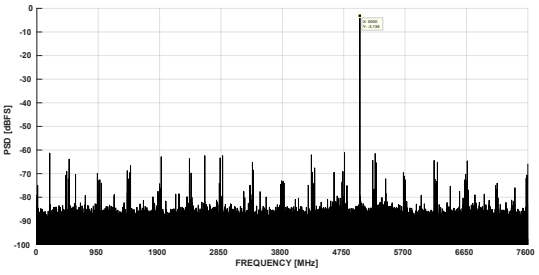


Fig 7-19. FFT at Fin = 5GHz, 15.2GSPS (0.8Vpp FS, -1dBFS)

CAE2300s
(Single Channel Mode)

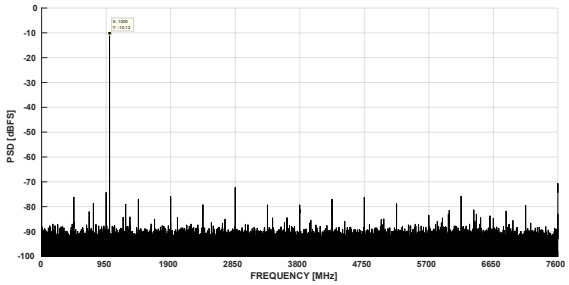


Fig 7-20. FFT at Fin = 1GHz, 15.2GSPS (0.8Vpp FS, -10dBFS)

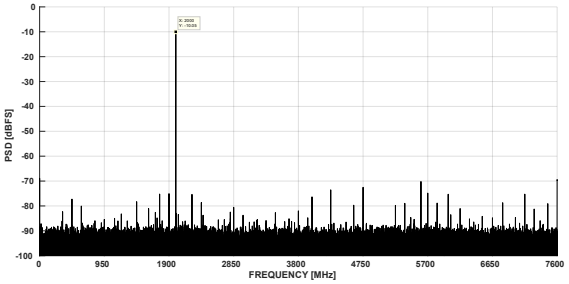


Fig 7-21. FFT at Fin = 2GHz, 15.2GSPS (0.8Vpp FS, -10dBFS)

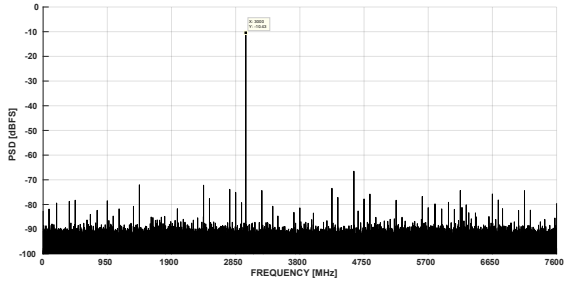


Fig 7-22. FFT at Fin = 3GHz, 15.2GSPS (0.8Vpp FS, -10dBFS)

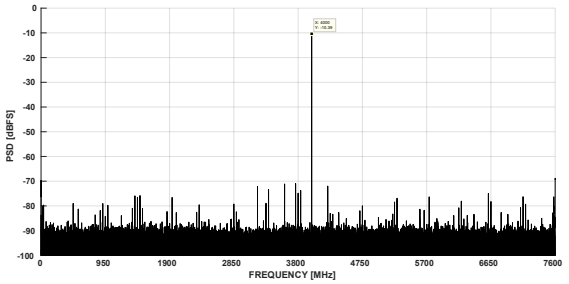


Fig 7-23. FFT at Fin = 4GHz, 15.2GSPS (0.8Vpp FS, -10dBFS)

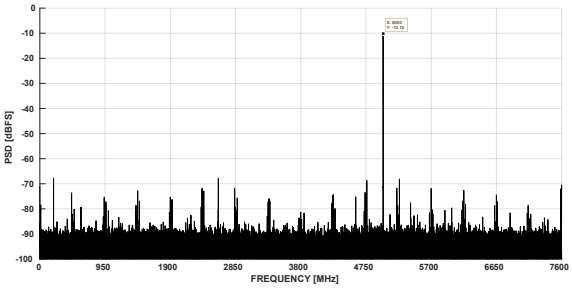


Fig 7-24. FFT at Fin = 5GHz, 15.2GSPS (0.8Vpp FS, -10dBFS)

CAE2400s
(Single Channel Mode)

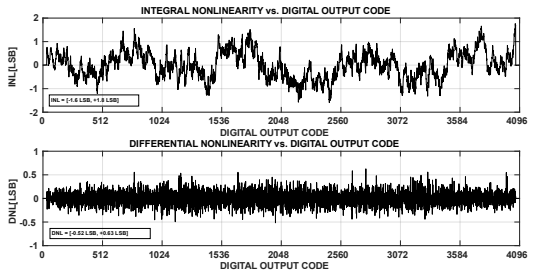


Fig 7-25. INL/DNL at Fin = 180MHz, 12GSPS (0.8Vpp FS)

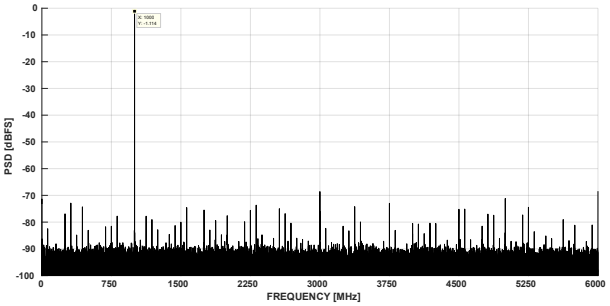


Fig 7-9. FFT at Fin = 1.09GHz, 12GSPS (0.8Vpp FS, -1dBFS)

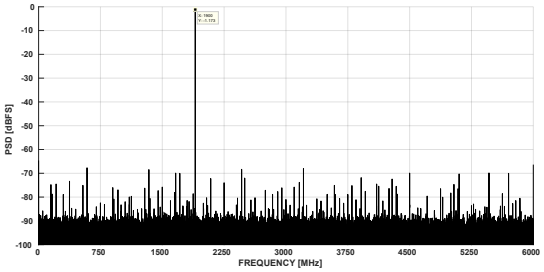


Fig 7-10. FFT at Fin = 1.9GHz, 12GSPS (0.8Vpp FS, -1dBFS)

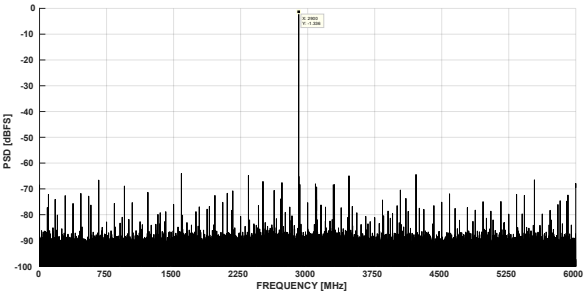


Fig 7-11. FFT at Fin = 2.9GHz, 12GSPS (0.8Vpp FS, -1dBFS)

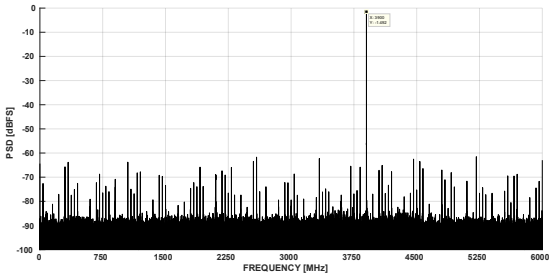


Fig 7-12. FFT at Fin = 3.9GHz, 12GSPS (0.8Vpp FS, -1dBFS)

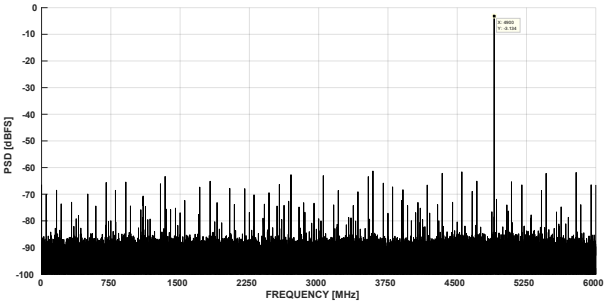


Fig 7-30. FFT at Fin = 4.9GHz, 12GSPS (0.8Vpp FS, -1dBFS)

CAE2400s
(Single Channel Mode)

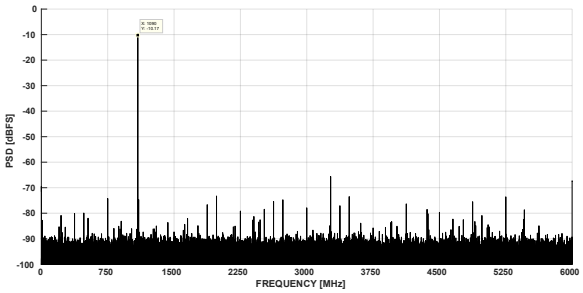


Fig 7-31. FFT at Fin = 1.09GHz, 12GSPS (0.8Vpp FS, -10dBFS)

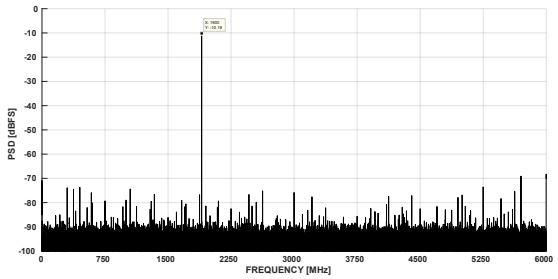


Fig 7-32. FFT at Fin = 1.9GHz, 12GSPS (0.8Vpp FS, -10dBFS)

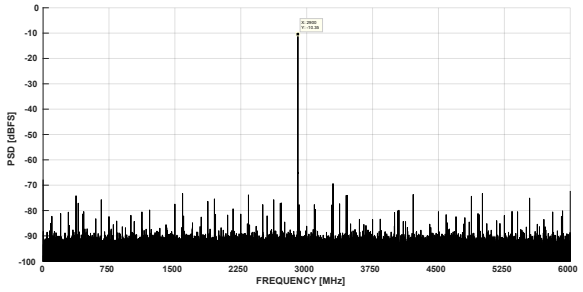


Fig 7-33. FFT at Fin = 2.9GHz, 12GSPS (0.8Vpp FS, -10dBFS)

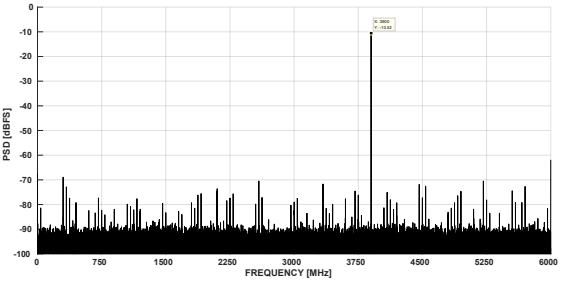


Fig 7-34. FFT at Fin = 3.9GHz, 12GSPS (0.8Vpp FS, -10dBFS)

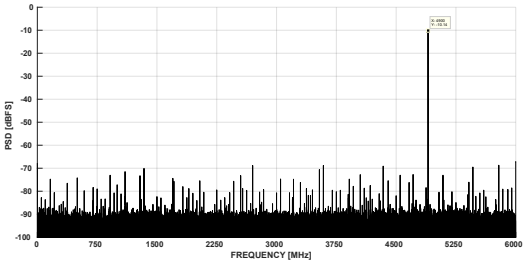


Fig 7-35. FFT at Fin = 4.9GHz, 12GSPS (0.8Vpp FS, -10dBFS)

8 Detailed Description

8.1 Overview

CAE2200S is a 12b high speed RF sampling ADC with maximum sampling rate of 20.8GSPS in single channel mode and maximum sampling rate of 10.4GSPS in dual channel mode, and maximum sampling rate of 5.2GSPS in quad channel mode.

CAE2300S is a 12b high speed RF sampling ADC with maximum sampling rate of 15.2GSPS in single channel mode and maximum sampling rate of 7.6GSPS in dual channel mode, and maximum sampling rate of 3.8GSPS in quad channel mode.

CAE2400S is a 12b high speed RF sampling ADC with maximum sampling rate of 12GSPS in single channel mode and maximum sampling rate of 6GSPS in dual channel mode, and maximum sampling rate of 3GSPS in quad channel mode.

The chip can be configured as single channel mode / dual channel mode / quad channel mode by SPI setting, which supports multiple channels or instantaneous wide bandwidth applications.

CAE2200S / **CAE2300S** / **CAE2400S** adopt JESD204B interface, with operating junction temperature of -40 to 115°C and use the package of Flip-Chip BGA 484 pins (19mm x 19mm).

8.2 Functional Block Diagram

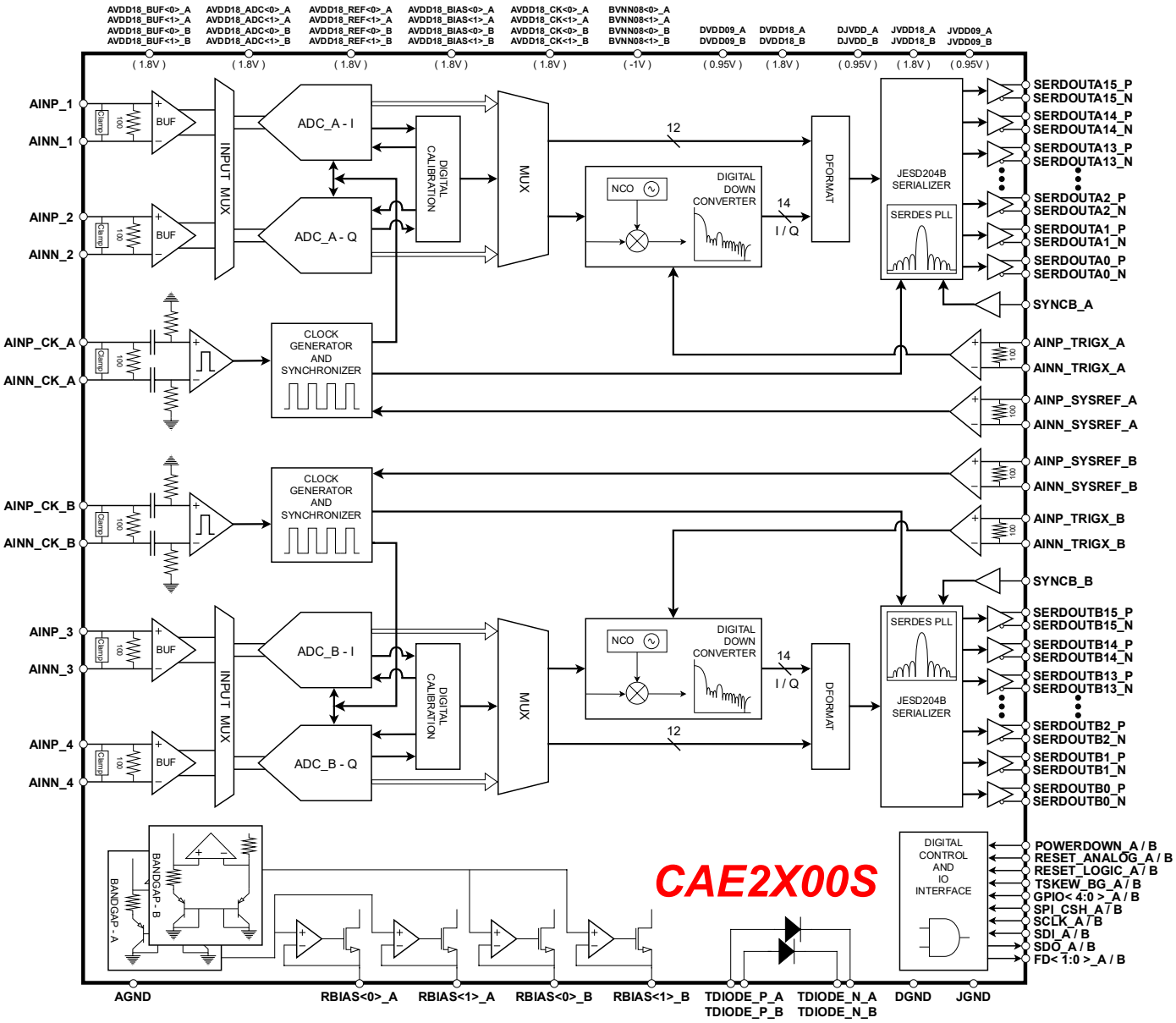


Fig 8-1. Functional Block Diagram

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